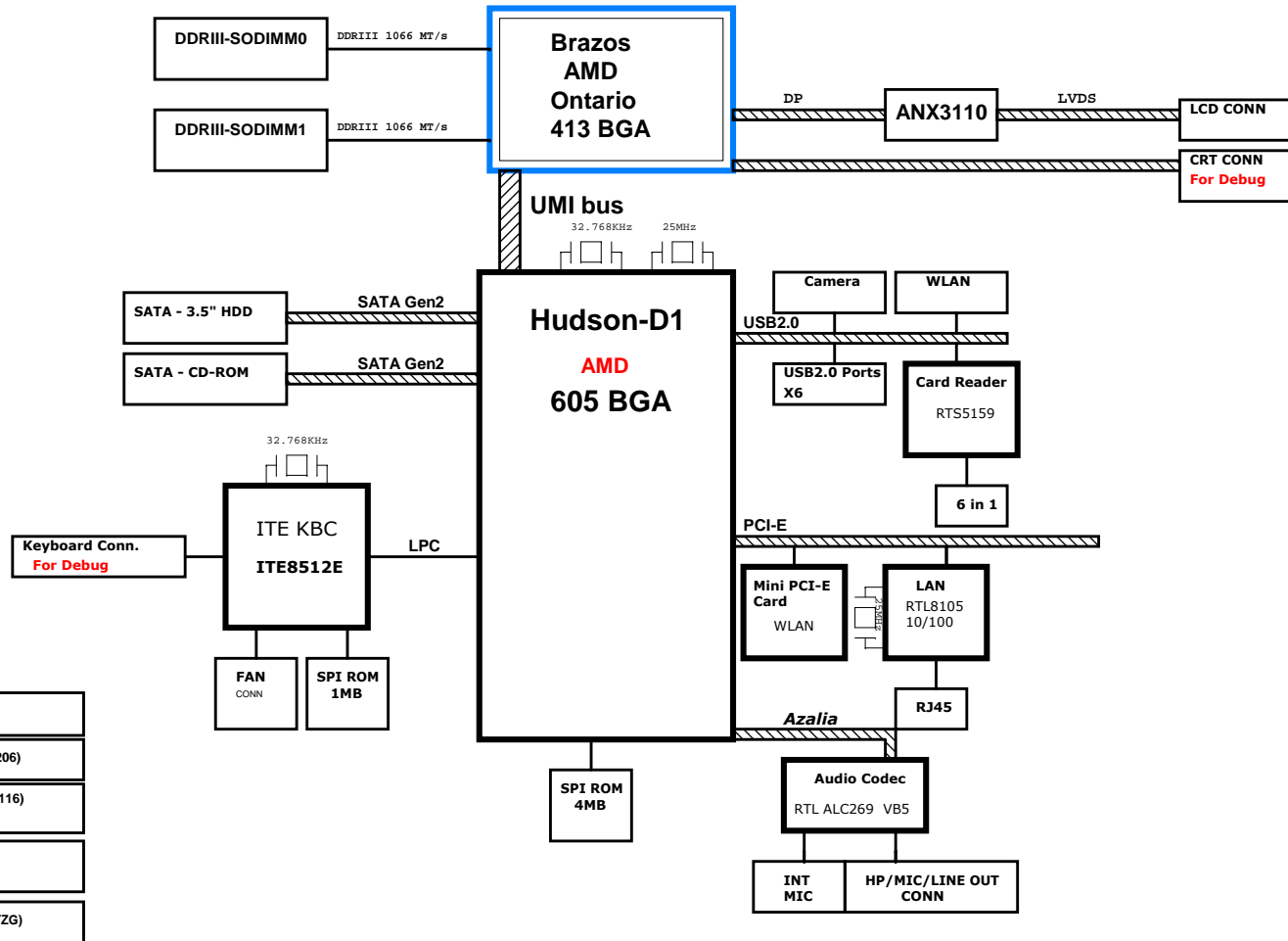


BRAZOS BLOCK DIAGRAM

PCB STACK UP

LAYER 1 : TOP
LAYER 2 :VCC
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 :GND
LAYER 6 : Bottom



| |
|--|
| CPU CORE(QZ8380) 1V_CPU(RT8209A) |
| System +5V/+3V (RT8206) |
| DDR_1.5VSUS (TPS51116) VCC1.5 (AO6402A) |
| 1.8_CPU (APL5930) VCC1.2 (APL5930) |
| HDD_12V(NCP1589MNTZG) |


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Schematic Page Description :

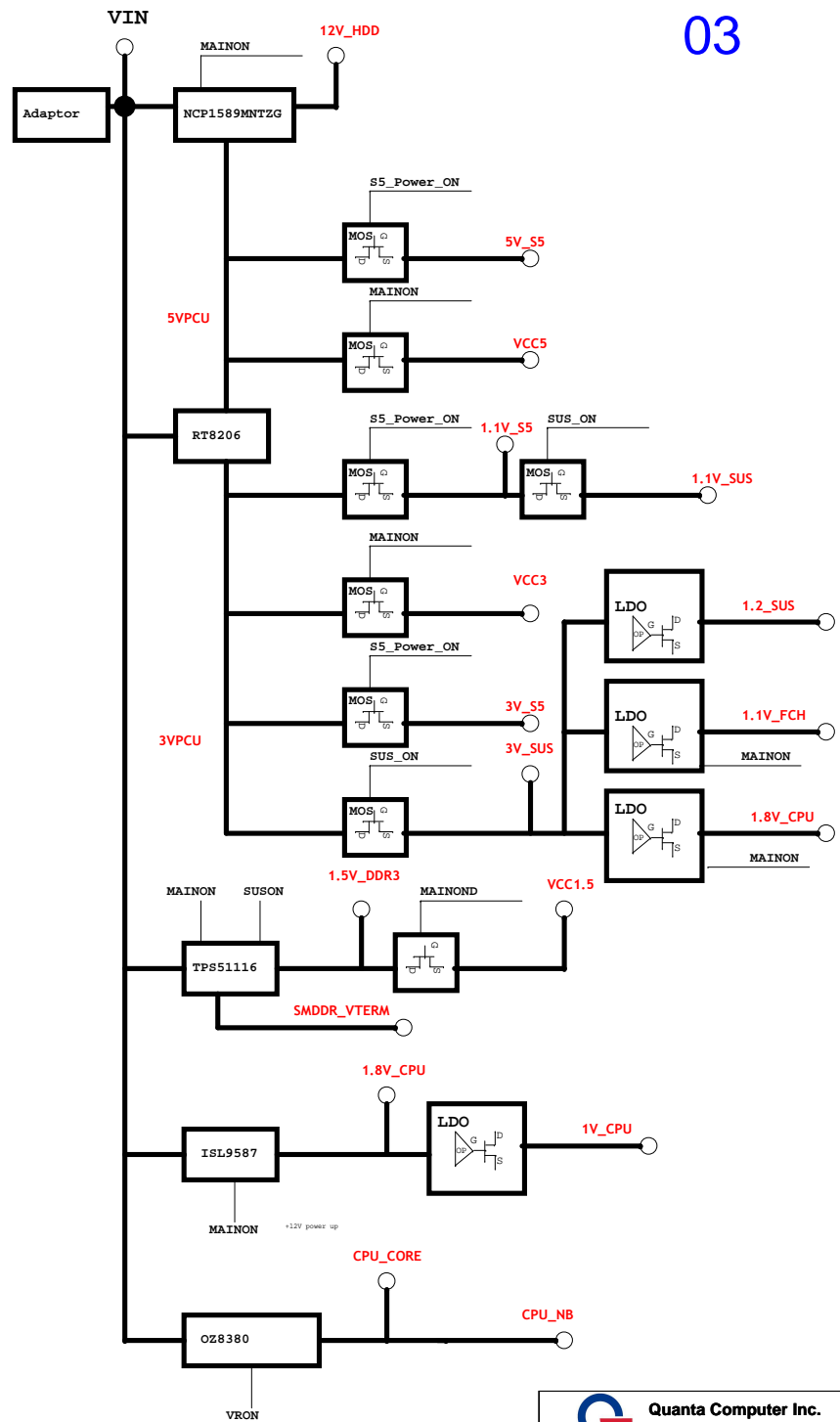
02

- | | |
|---------------------------------|---------------------------------|
| 01--Block Diagram | 20--Panel (LVDS) |
| 02--Page list | 21--Audio Codec(ALC269) |
| 03--Power Map | 22--LAN RTL8105 |
| 04--Power Sequence 1/2 | 23--CARD READER RTS5159 |
| 05--Power Sequence 2/2 | 24--SATA HDD/ODD/FAN/Mini PCIE |
| 06--Clock | 25--USB/CCD/CRT |
| 07--SMBus Block Diagram | 26--EC ITE 8512E/FLASH |
| 08--GPIO list | 27--FT1 CPU HT & DEBUG |
| 09--ONTARIO MEM/PCIE I/F(1/3) | 28--DVI Scaler RTL2281 |
| 10--ONTARIO DISPLAY/CLK/MI(2/3) | 29--ACIN HDD12V(NCP1589) |
| 11--ONTARIO POWER/DECOUP(3/3) | 30--3VPCU 5VPCU(RT8206) |
| 12--HUDSON PCIE/PCI/CLOCK/(1/5) | 31--1.5V_DDR3(TPS51116) |
| 13--HUDSON SATA/DEBUG IO/S(2/5) | 32--1V_CPU(RT8290A) |
| 14--HUDSON GPIO/USB/AUDIO(3/5) | 33--LDO VCC1.2 1.1V_S5 1.8V_CPU |
| 15--HUDSON Power(4/5) | 34--CPU(OZ8380) |
| 16--HUDSON GND(5/5) | 35--DISCHARGE |
| 17--HUDSON-STRAPS/PWRGD | 36--CHANGE LIST |
| 18--DDR3 CHA DIMM 0 | |
| 19--DDR3 CHB DIMM 1 | |

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|---|------------------------|-----------------------------|---------|
|  | | Quanta Computer Inc. | |
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| Page List | | A1 | |
| Date: | Monday, April 25, 2011 | Sheet | 2 of 37 |

| Power Rail | Destination | Voltage | S0 Current |
|-------------|---|--|----------------------------|
| CPU_CORE | FT1: Core power supply | 0.65V-1.3V | 11A |
| CPU_NB | Northbridge power supply | 0.5 V-1.3V | 10A |
| 1V_CPU | PCIe, , Memory and LTDP cores | 1V | 8A |
| 1.8V_CPU | (PCIe, LTDP, GPIOs and PLLs) FCH : | 1.71V-1.8V-1.89V 1.71V-1.8V-1.89V | 6.5A 0.196A |
| 1.5V_DDR3 | DDRIII CPU I/O Voltage for DDRIII | 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V | 5A 3A |
| SMDDR_VTERM | DDRIII Terminator: | 0.75V | 1A |
| 1.1V_FCH | FCH | 1.1V | 5A |
| 1.1V_S5 | FCH | 1.1V | 2A |
| VCC1.2 | Scaler | 1.2V | 1A |
| VCC1.5 | Mini PCIE : +1.5V(WLAN) | 1.5V | 3A |
| VCC3 | general purpose I/Os FCH: I/O buffer voltage FCH: Display DAC Analog power IDT 92HD80 : DVDD Mini PCIE : +3.3V(WLAN) CAREMA | 0.925 V/0.85 V 3.14V-3.3V-3.47V | 8.8A 0.357A 0.069A |
| VCC5 | FCH: Core well Ref. voltage SATA ODD SATA HDD(2.5" x SSD) LCD Panel | 4.75V-5V-5.25V | 0.001A 2.5A |
| 5V_SUS | USB: x 9 ports | 5V | 5A |
| 12V_HDD | HDD FAN_CPU | 12V | 2A |
| 3V_S5 | FCH : Power Management Engine FCH : Suspend well I/O Buffer FCH : HD Audio controller LAN 8105E : VDD EC(IT8512) : VSTBY SPI FLASH ROM | 3.14V-3.3V-3.47V 3.14V-3.3V-3.47V 3.14V-3.3V-3.47V | 0.086A 0.168A 0.006A |
| 5V_S5 | FCH : Suspend well Ref. Voltage | 4.75V-5V-5.25V | 0.001A |
| 3VPCU | I/O/FCH/EC | 3V | 5A |
| 5VPCU | I/O/FCH/EC | 5V | 5A |
| VIN | INVERTER : Vin | 19V | 1A(12.7w) |



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```

EC
FCH SUS,
Sys Management, FCH Resume Well, Intel HD Audio, USB, WLAN,
Sys Management, FCH Resume Well, Intel HD Audio, USB, WLAN,
FCH
FCH
USB
DDR3 Memory
DDR3 Memory
SATA, PCI REF
PCI Express*, SATA, HV CMOS, CRT, Band Gap voltages, Intel HD Audio
mini PCIe, Intel HD Audio
PCH core, PCH PLL voltages, PCH CLK Buffer, SATA, USB, PCH fuses, Display Link, Display Port, PCIe
LVDS0, SFR, FLASH
CPU VTT, FIDPES, DIML VCCT1ADDR, PCH DIMLPGH V_CPU_IO
mini PCIe, Intel HD Audio

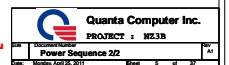
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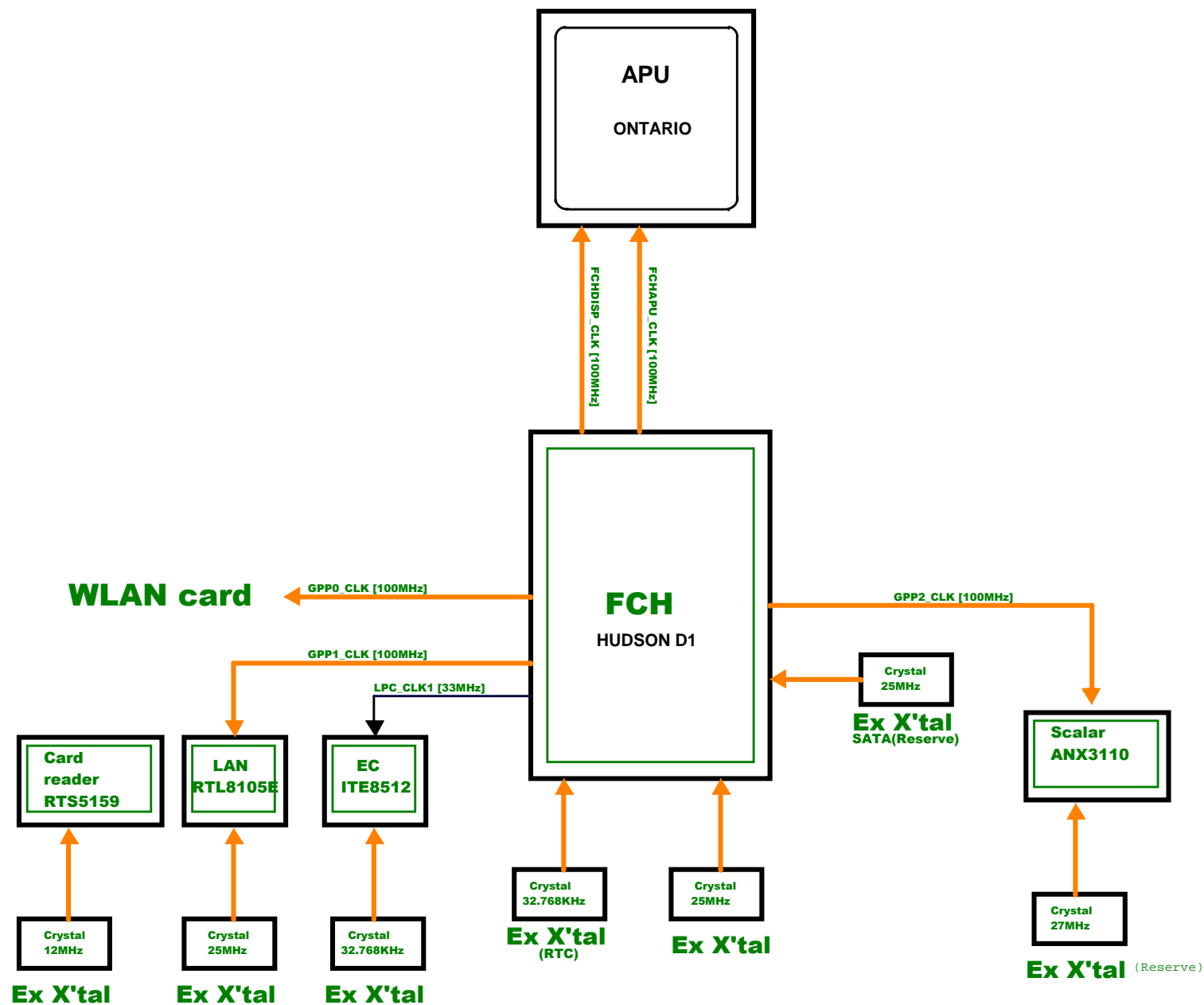
3V_SUS/1.1V_SUS/1.5V_DDR3/5V_SUS

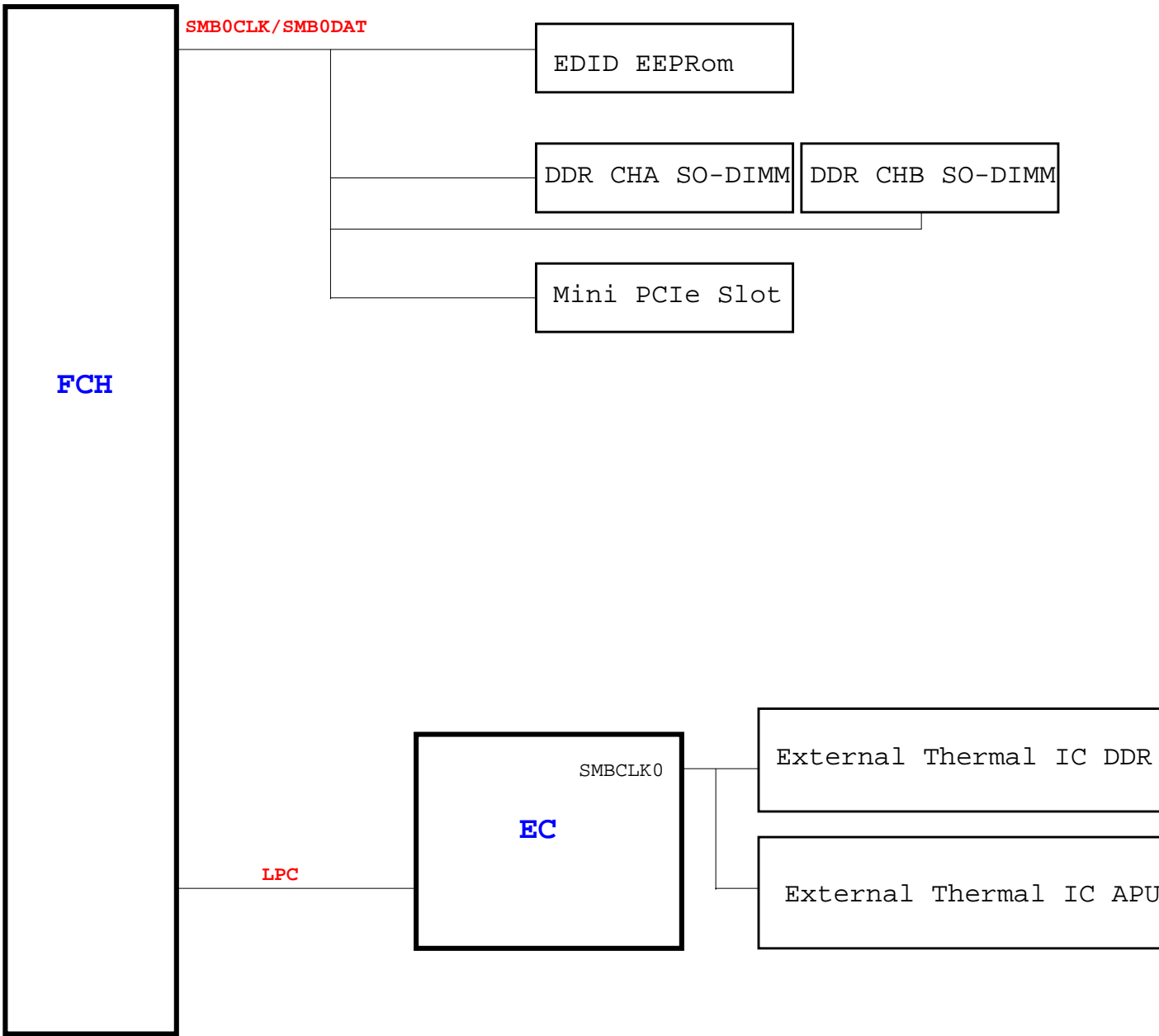
VCC5/VCC3/1.8V_CPU/1.1V_FCH/1V_CPU



05



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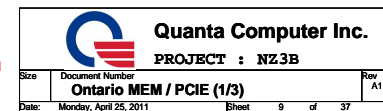


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| NAME | GPIO/PIN | I/O | DESCRIPTION | ACTIVE |
|------|----------|-----|-------------|-------------------------------|
| | | I | | INITIAL : HIGH / ACTIVE : LOW |
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| NAME | GPIO/PIN | I/O | DESCRIPTION | ACTIVE |
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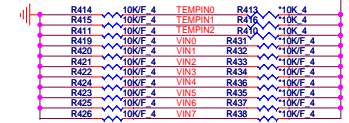
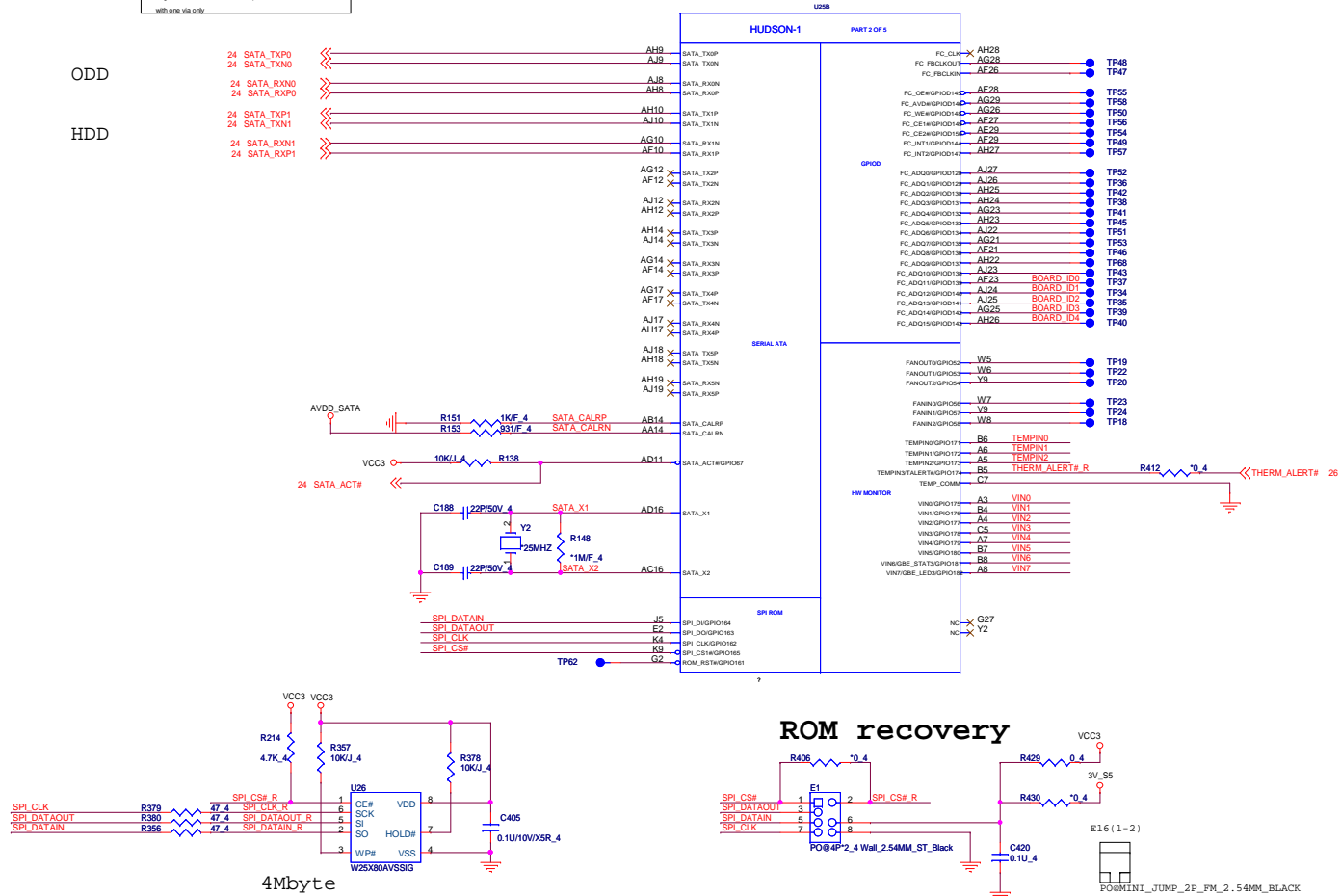
CONFIDENTIAL



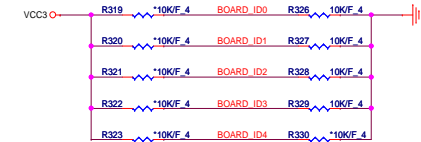
SATA trace should use only 1via on the trace.
customers can use 2vias with GND via within 150mils of
signal via as long as they can ensure that their platform
meets SATA logo requirements. Return loss is expected
to get affected with 2 vias. AMD platforms are validated
with one via only.

ODD

HDD



NOTE: ROUTE TEMP_C0MM
AS A 10K11 TRACE
PLACE Q600 UNDER D100
SCDS_IMAGE[clipboard_0_0.jpg][146]153



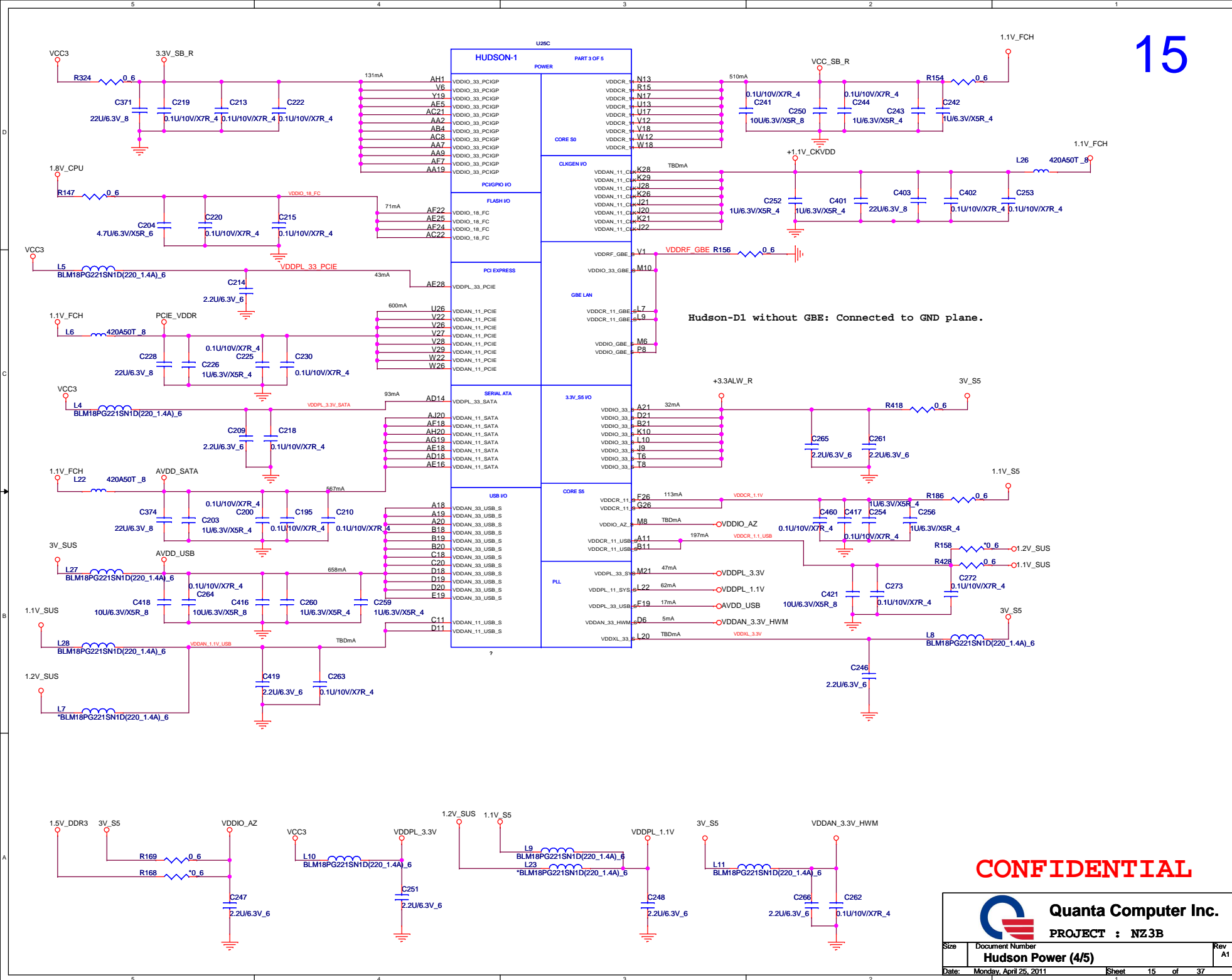
| Model | ID2 | ID1 | ID0 |
|---------------|-----|-----|-----|
| Kallang DC/SC | 0 | 0 | 0 |
| Kallang DG | 0 | 0 | 1 |

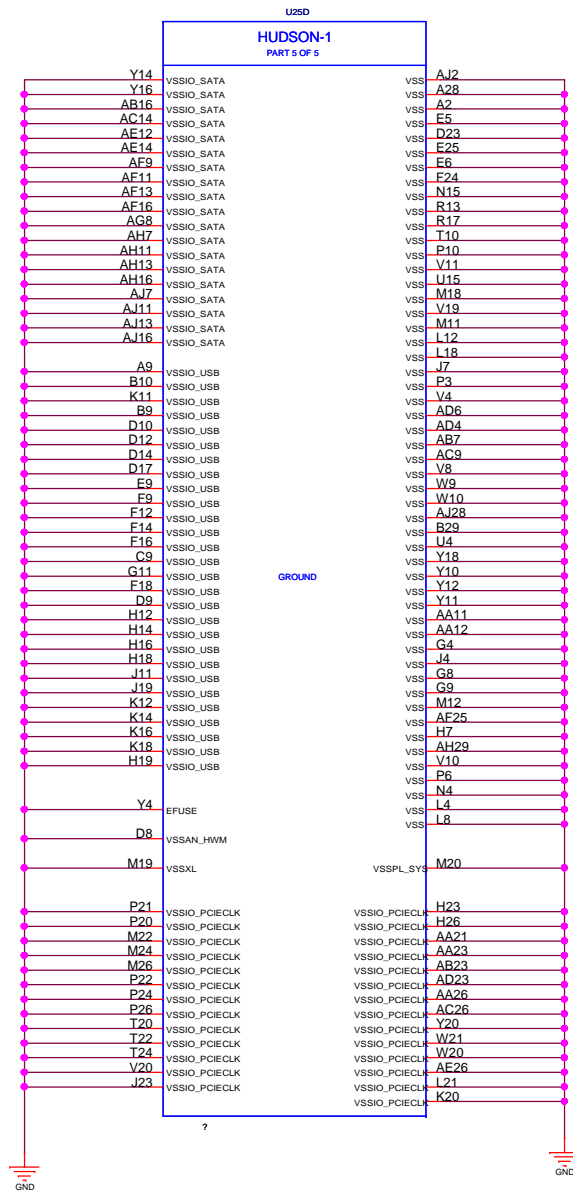
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| | | |
|-------|---------------------------|----------------|
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| | Hudson Power (4/5) | A |
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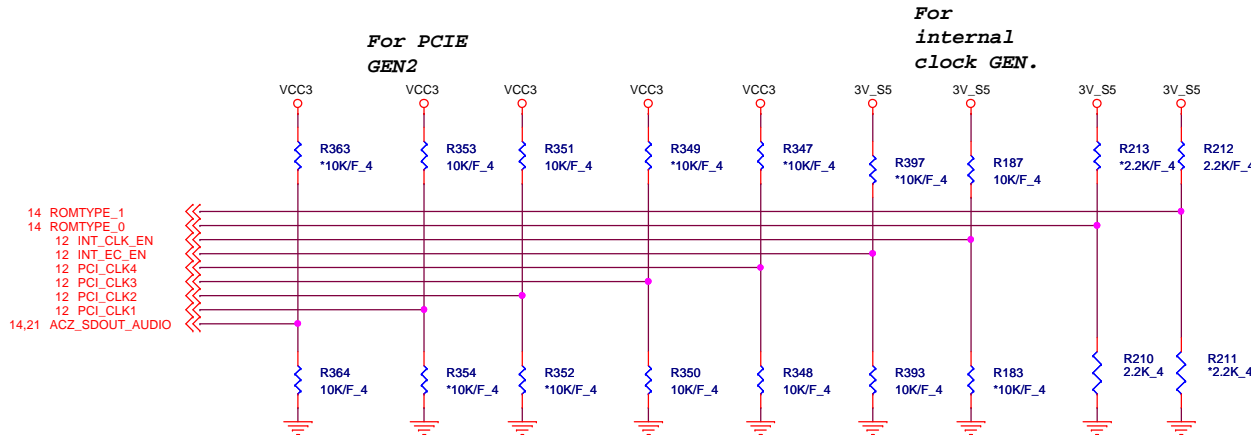
| | | |
|-------|-------------------------|----------------|
| Size | Document Number | Rev |
| | Hudson Gnd (5/5) | A1 |
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REQUIRED STRAPS



OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

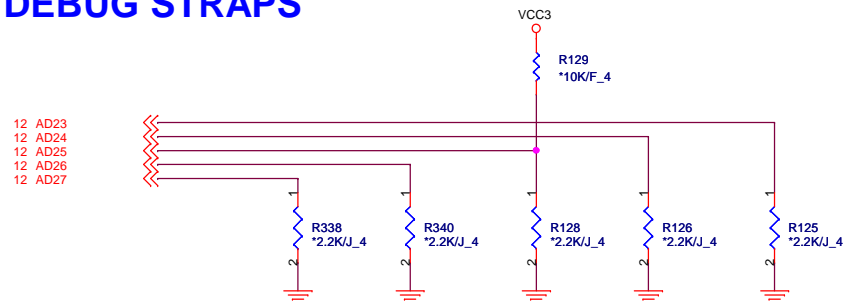
17



| | ACZ_SDOUT | PCI_CLK1 | PCI_CLK2 | PCI_CLK3 | PCI_CLK4 | INT_EC_EN | INT_CLK_EN | ROMTYPE_1/0 |
|------------------|-----------------------------|----------------------------|----------------------------------|--------------------------------|------------------------------|---------------------------------|--------------------------------|---------------------------------------|
| PULL HIGH | LOW POWER MODE | ALLOW PCIE Gen2 DEFAULT | Watchdog Timer Enable DEFAULT | USE DEBUG STRAPS | non_Fusion CLOCK MODE | INTERNAL EC ENABLED DEFAULT | INT. CLKGEN ENABLED DEFAULT | H, H=Reserved H, L=SPI ROM DEFAULT |
| PULL LOW | PERFORMANCE MODE DEFAULT | FORCE PCIE Gen1 | Watchdog Timer Disable | IGNORE DEBUG STRAPS DEFAULT | Fusion CLOCK MODE DEFAULT | INTERNAL EC DISABLED DEFAULT | EXT. CLKGEN ENABLE | L,H=LPC ROM L, L=FWH ROM |

internal have
pull Hi 10K

DEBUG STRAPS



| | PCI_AD27 | PCI_AD26 | PCI_AD25 | PCI_AD24 | PCI_AD23 |
|------------------|------------------------|--------------------------------|-----------------------|--|---------------------------------|
| PULL HIGH | USE PCI PLL DEFAULT | DISABLE ILA AUTORUN DEFAULT | USE FC PLL DEFAULT | DISABLE I2C ROM DEFAULT | DISABLE PCI MEM BOOT DEFAULT |
| PULL LOW | BYPASS PCI PLL | ENABLE ILA AUTORUN | BYPASS FC PLL | ENABLE I2C ROM use REQ3# as SDA use GNT3# as SCL | ENABLE PCI MEM BOOT |

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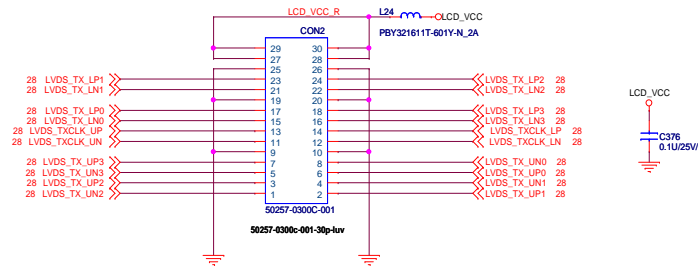
Quanta Computer Inc.
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Size Document Number
SB820M-STRAPS/PWRGD Rev A1

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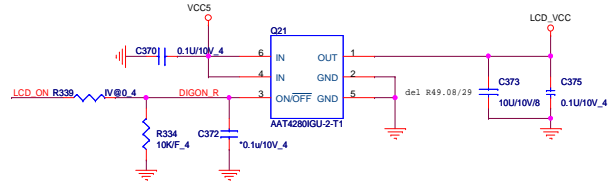
LCD CONNECTOR

20

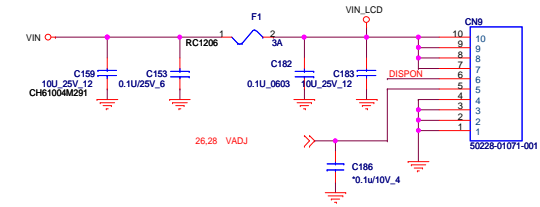
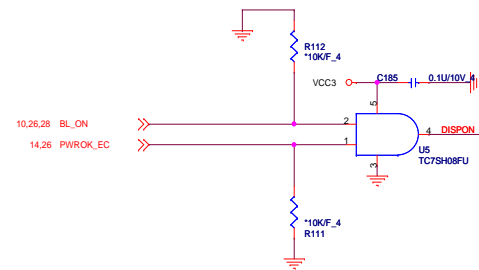


TO INVERTER POWER

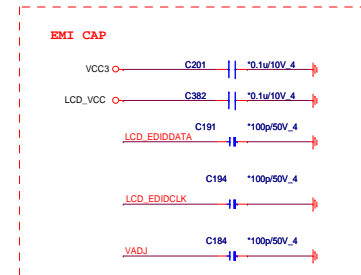
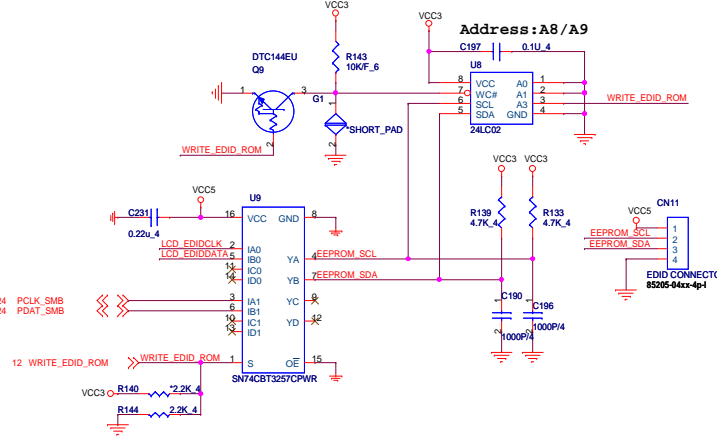
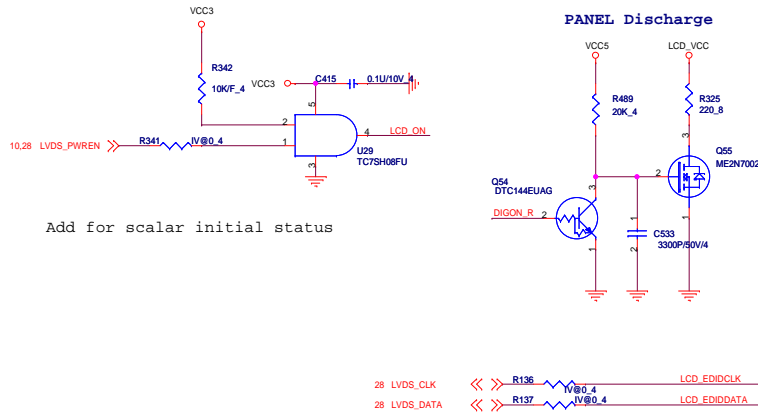
PANEL VCC CONTROL



PANEL BACKLIGHT CONTROL

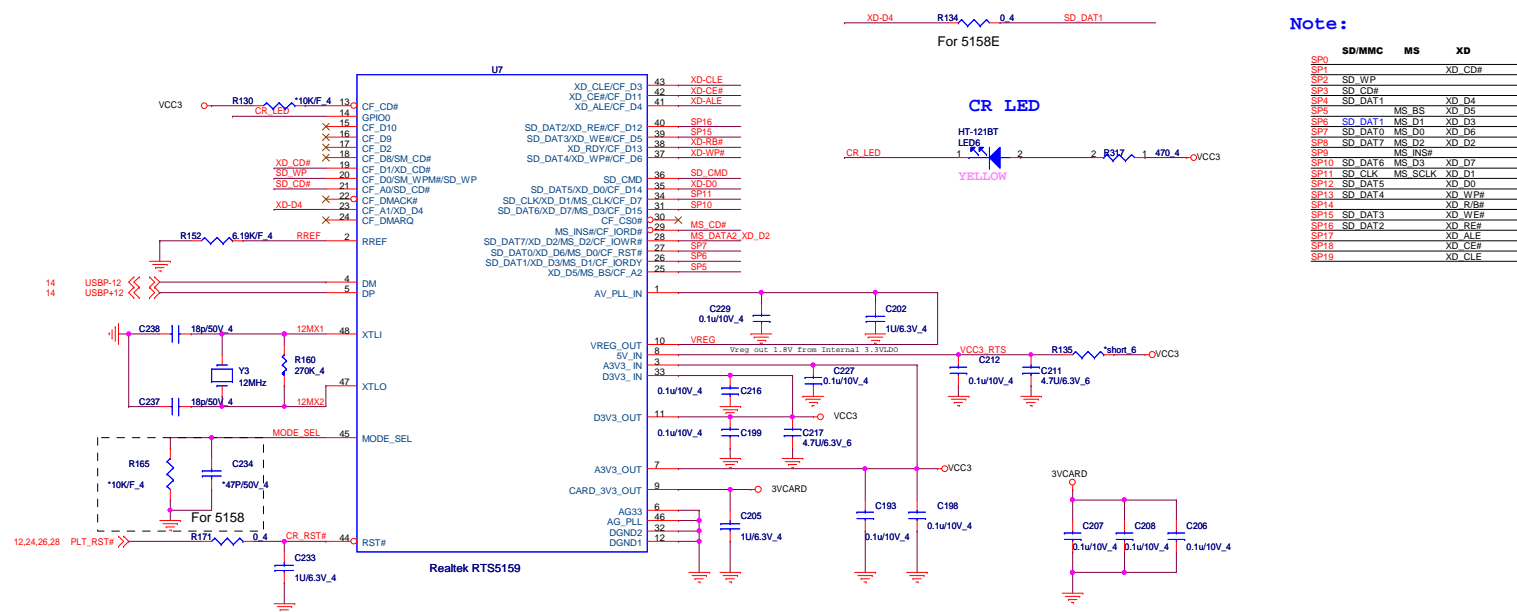


EEPROM IIC Selection PANEL EDID DATA

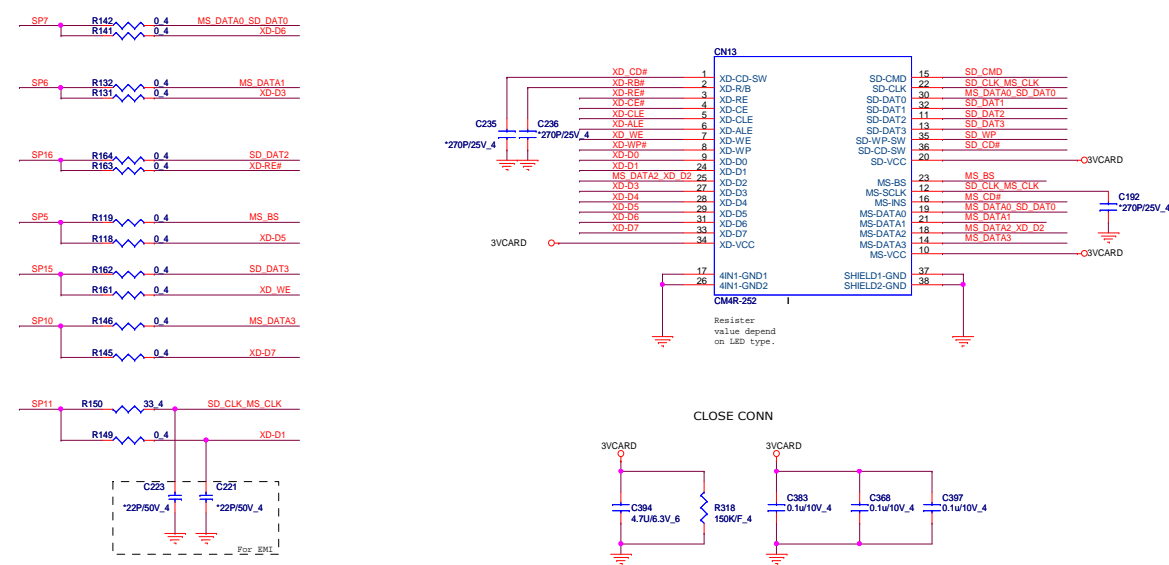


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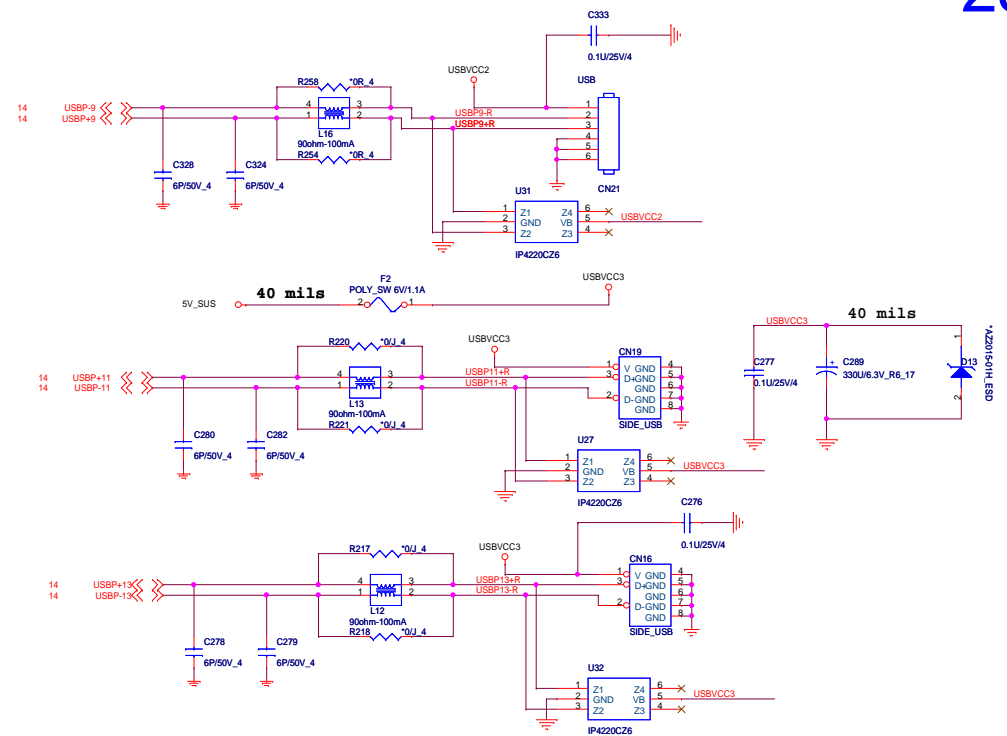
Card reader RTS5159



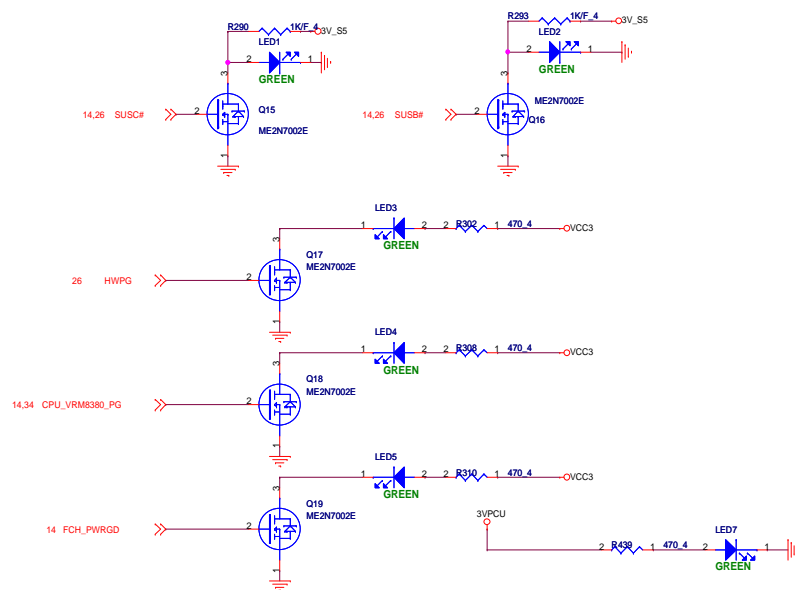
6 IN1 CARD READER
XD, MMC/SD/SDHC, MS/MSP



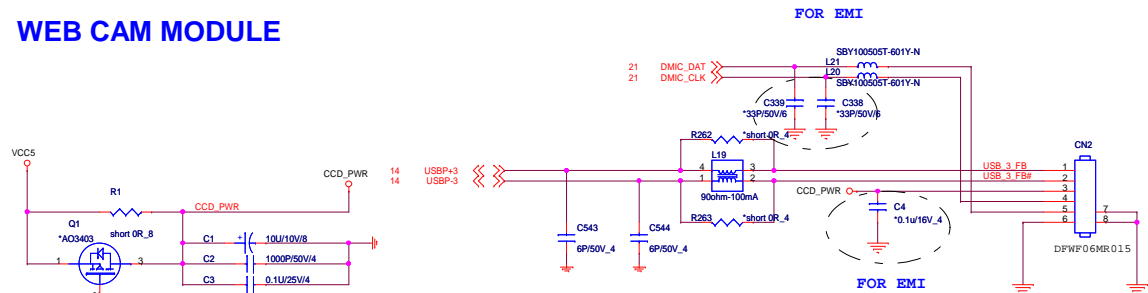
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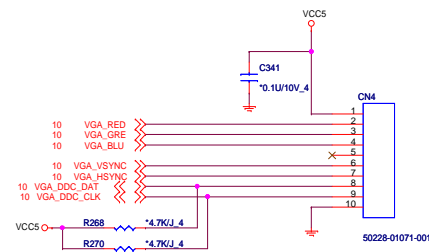
LED STATUS FOR DEBUG

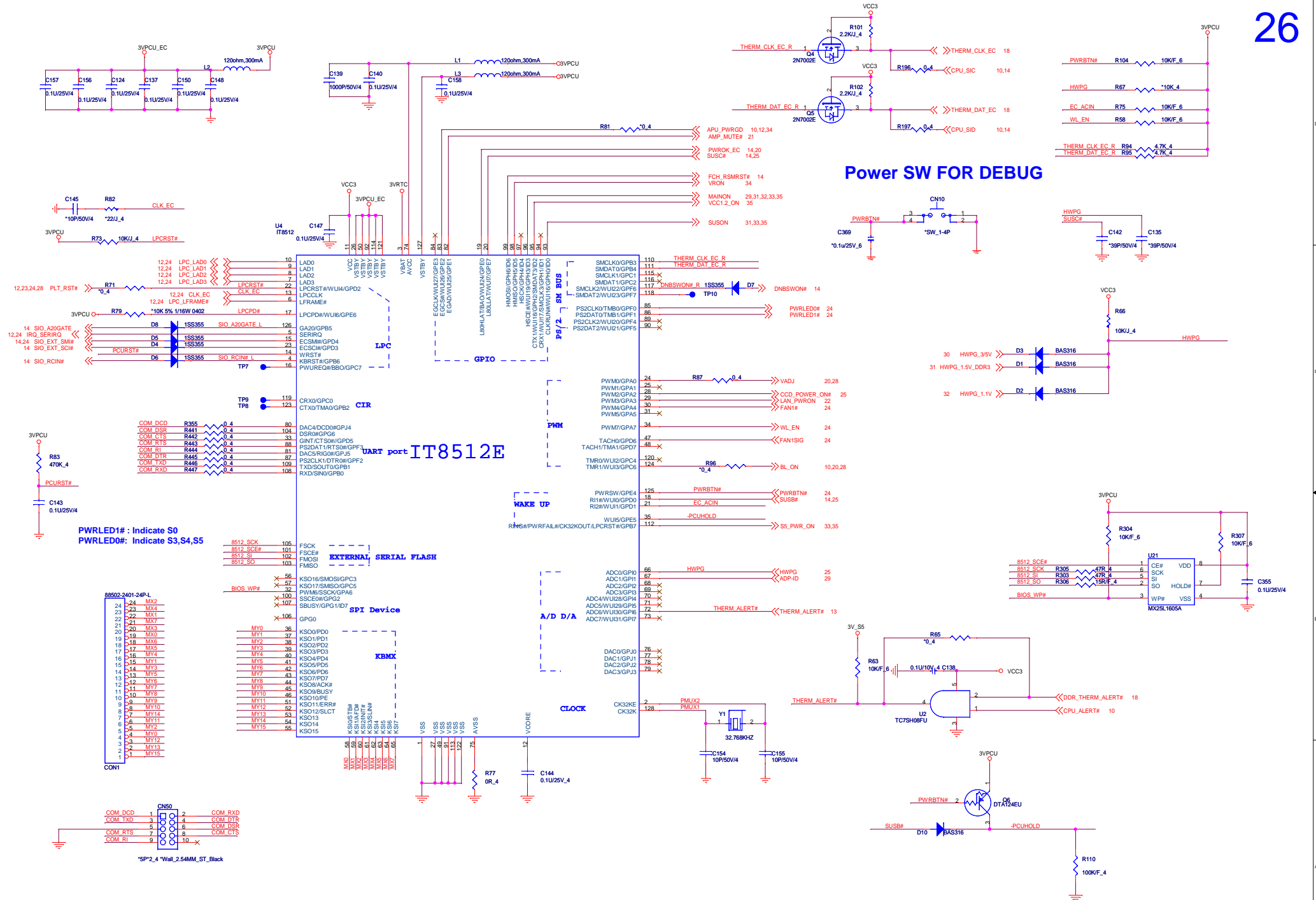


WEB CAM MODULE



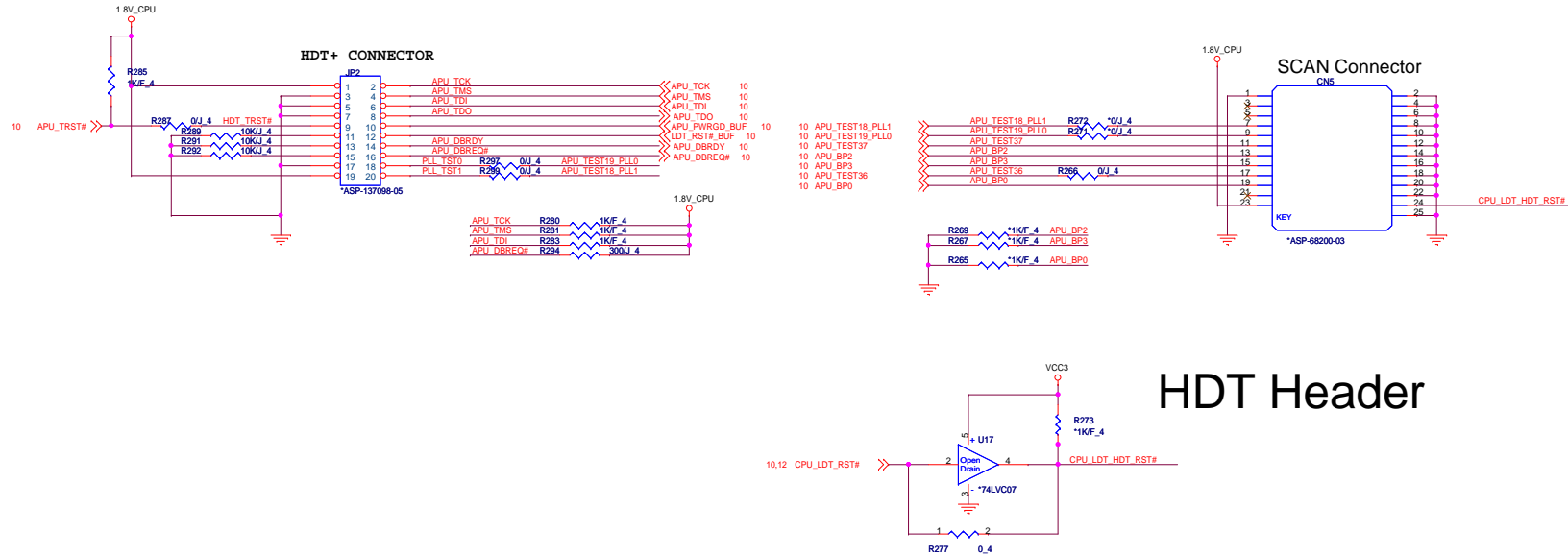
UMA CRT FOR DEBUG



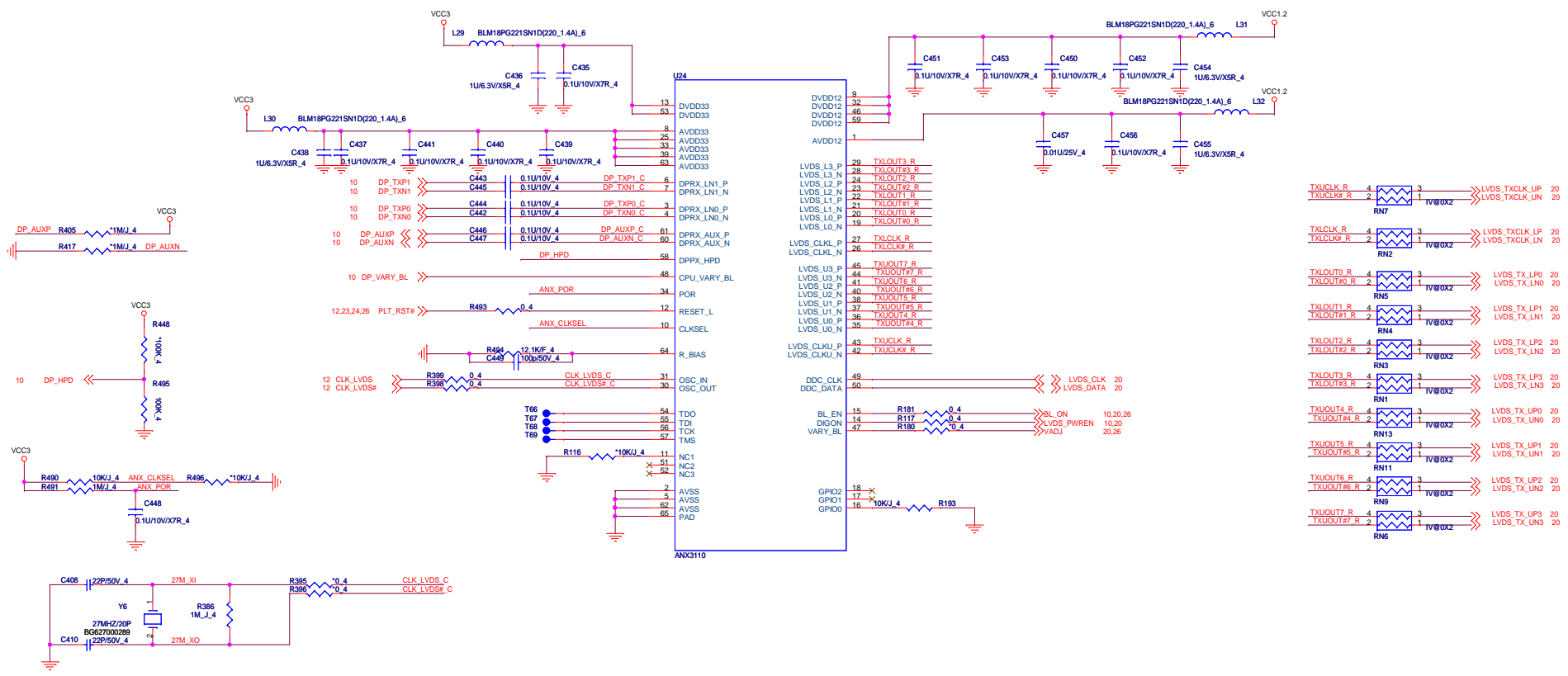


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Place in Top side



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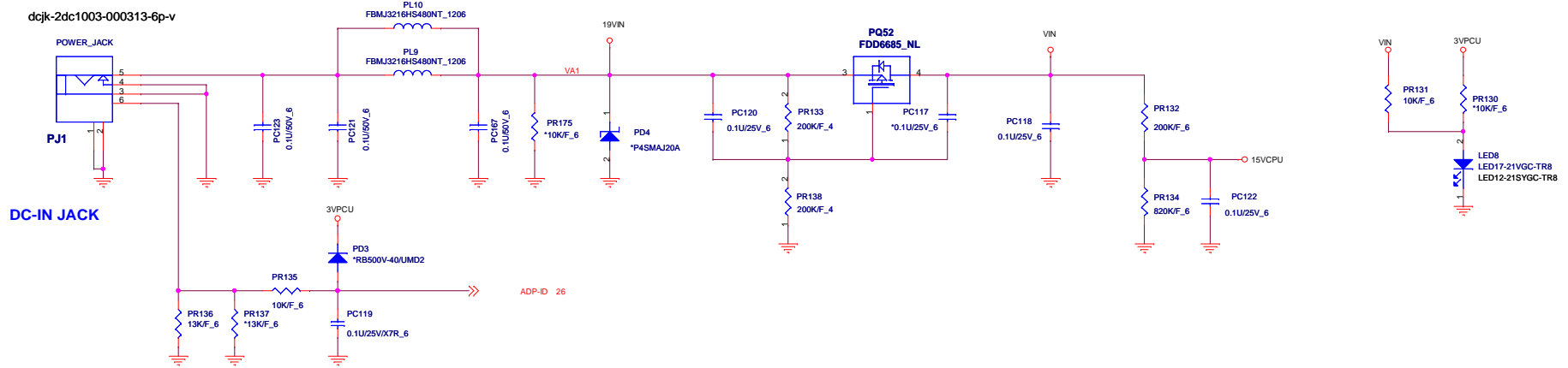


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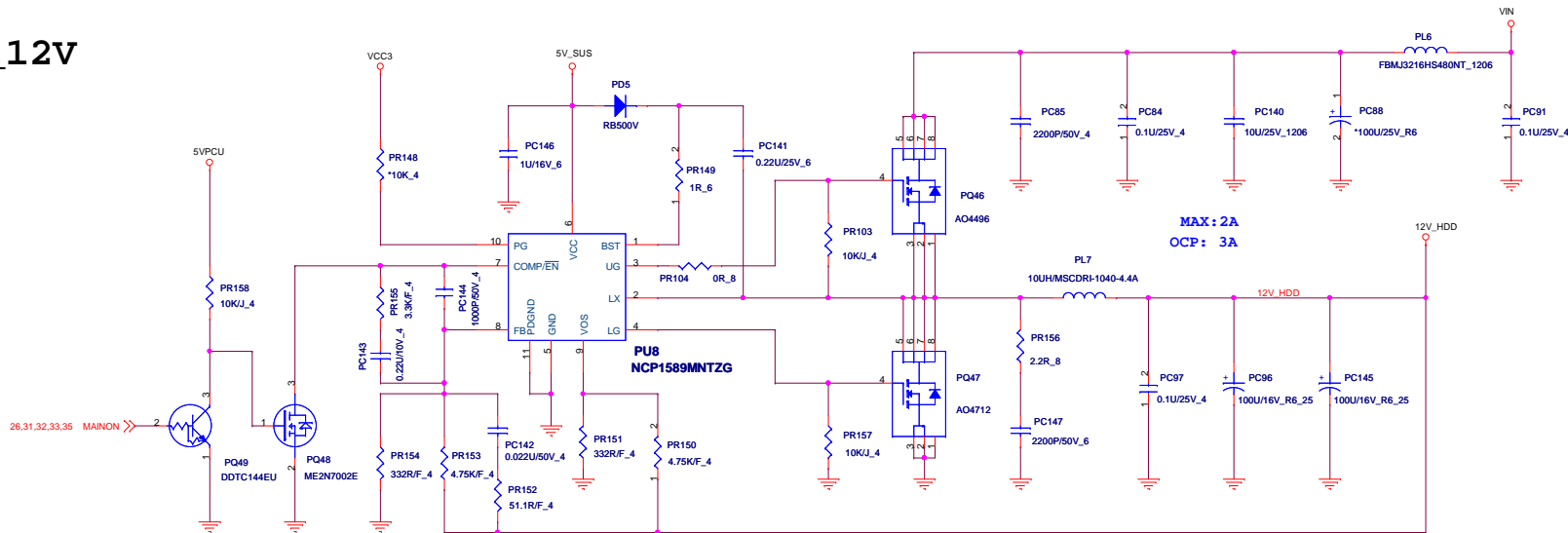
DC IN JACK

ramp-up time for all power rails
50 us <All power rails except 5V_S5 <40 ms
100 us <5V_S5<40 ms


29



HDD_12V



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| | | | | |
|--|--|------------------------------|-----------------|-----|
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Place these CAPs
close to FETs

Place these CAPs
close to FETs

5VPCU +/- 5%
Countinue current:4.9A
Peak current :6A
OCP minimum :7.5A

3VPCU +/- 5%
Countinue current:5.1A
Peak current:6A
OCP minimum 7.5A

AO4712 Rdsn=18mOhm
5VPCU OCP:7.5A 400K

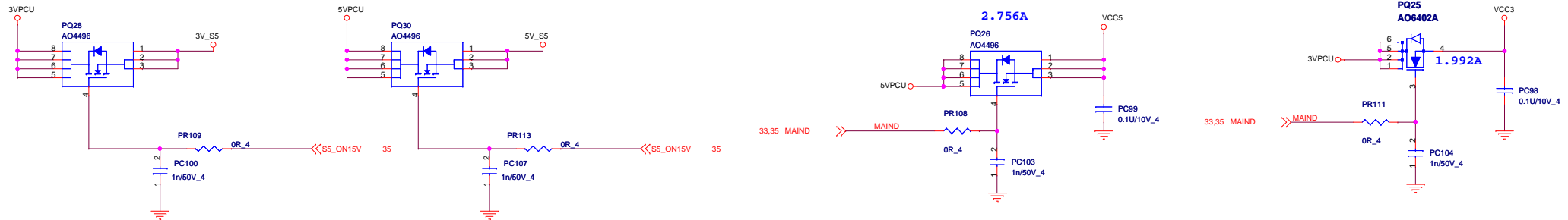
$L(\text{ripple current})$
 $= (19-5) \times 5 / (3.8 \mu \times 400 \times 19) \approx 2.4A$
 $I_{ocp} = 7.5 - (2.4/2) \approx 6.3A$
 $V_{th} = 6.3A \times 18m\Omega = 113.4mV$
 $R(I_{lim}) = (113.4mV \times 10) / 5\mu A = 226.8K$

Output1 -- 5V fix. FB1 to GND.

For MAX17020 use

AO4712 Rdsn=18mOhm
3VPCU OCP:7.5A 500K

$L(\text{ripple current})$
 $= (19-3.3) \times 3.3 / (3.8 \mu \times 500 \times 19) \approx 1.44A$
 $I_{ocp} = 7.5 - (1.44/2) \approx 6.78A$
 $V_{th} = 6.78A \times 18m\Omega = 122.04mV$
 $R(I_{lim}) = (122.04mV \times 10) / 5\mu A = 244K$

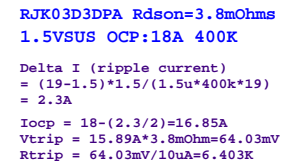



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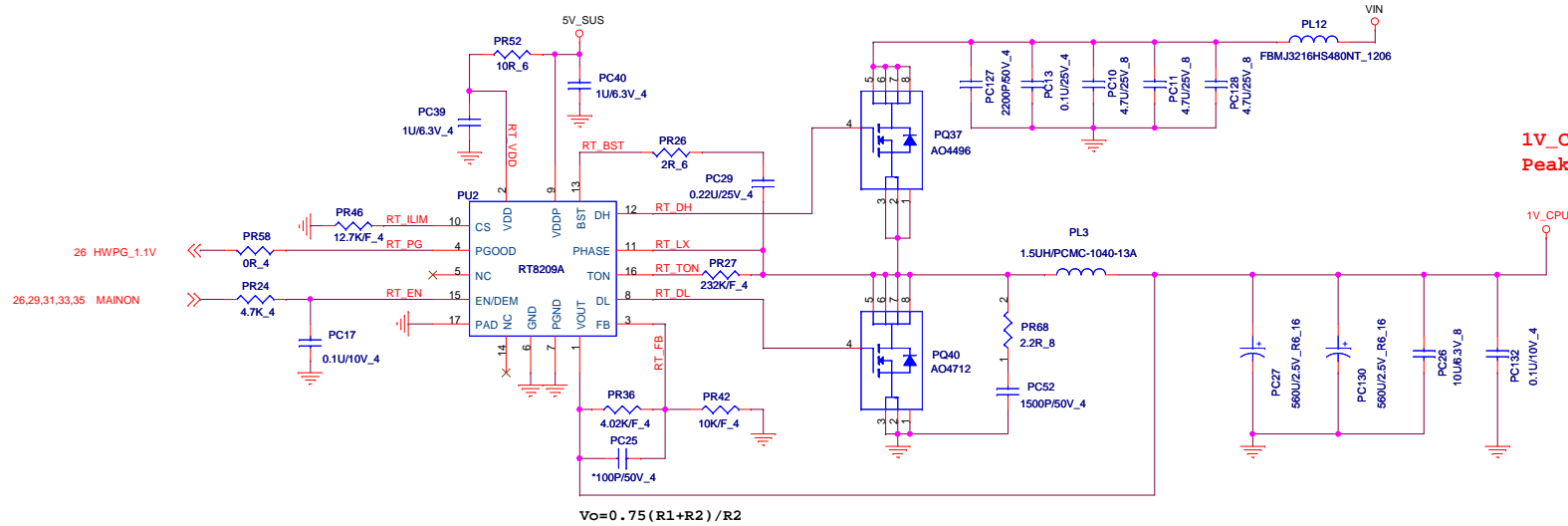


Quanta Computer Inc.
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|-------|------------------------|----------------|
| | | A1 |
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| | | |
|--|-----------------|-----------|
|  Quanta Computer Inc. PROJECT : NZ3B | | Rev A1 |
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| Date: Monday, April 25, 2011 | Sheet 31 of 37 | |



1V_CPU Volt: 1.05V +/- 5%
Peak current: 8A

RJK03D3DPA Rdson=18mOhm
1V_CPU OCP:10A 333K

L(ripple current)
= (19-1.05)*1.05 / (1*333k*19) ~ 2.98A
Iocp = 10 - (2.98/2) ~ 8.51A
Vcs = 8.51A * 18mOhm = 153.18mV
R(ILim) = 153.18mV/10uA = 15.4K

$$Vo = 0.75 (R1 + R2) / R2$$

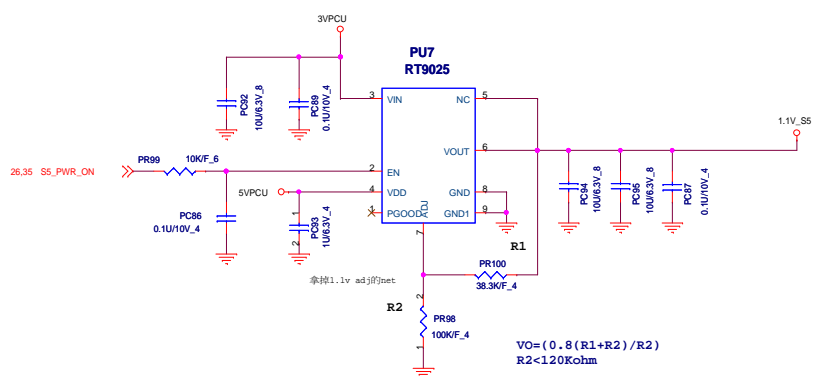
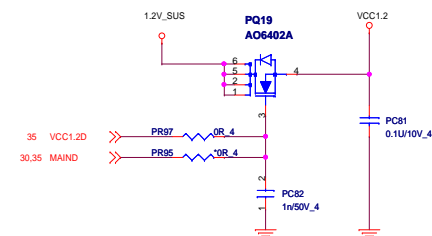
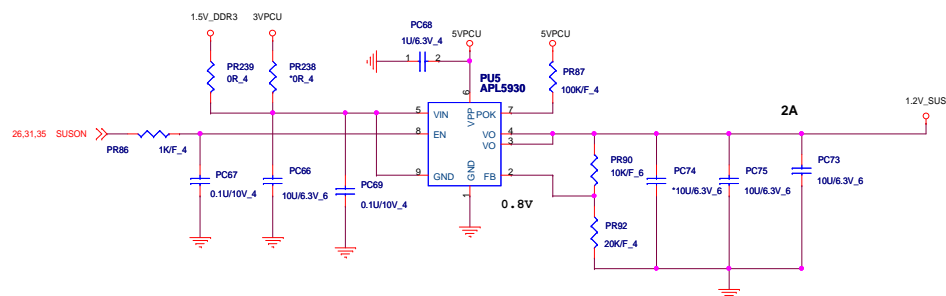
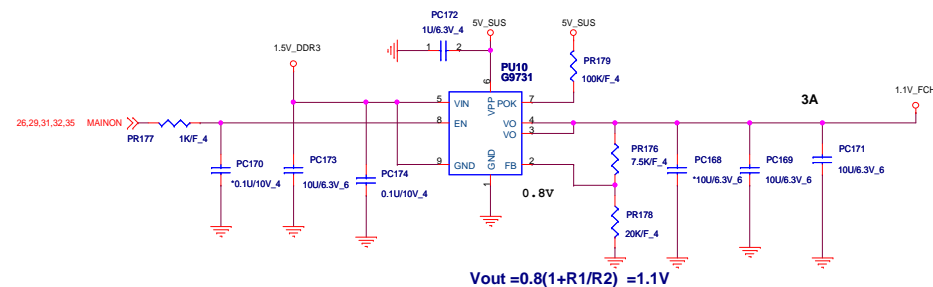
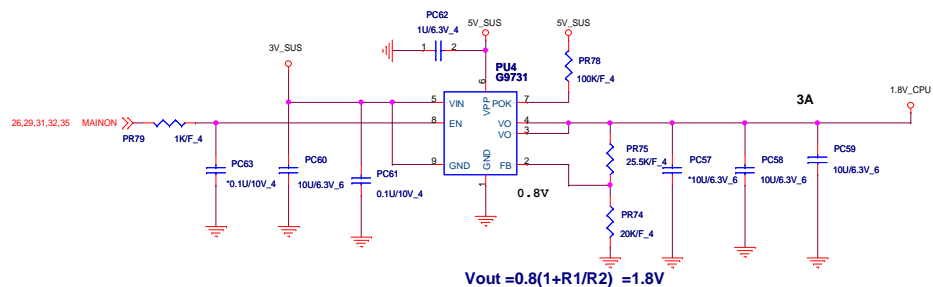
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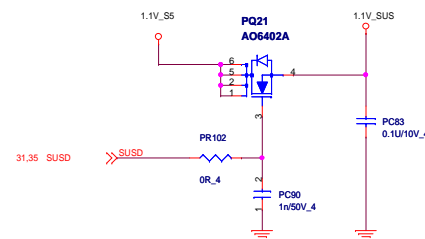
Quanta Computer Inc.

PROJECT : NZ3B

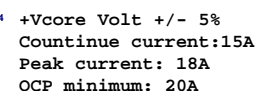
| Size | Document Number | Rev |
|-------|------------------------|----------------|
| | | A1 |
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1.1 Volt +/- 5%
Continuous current: 0.2A

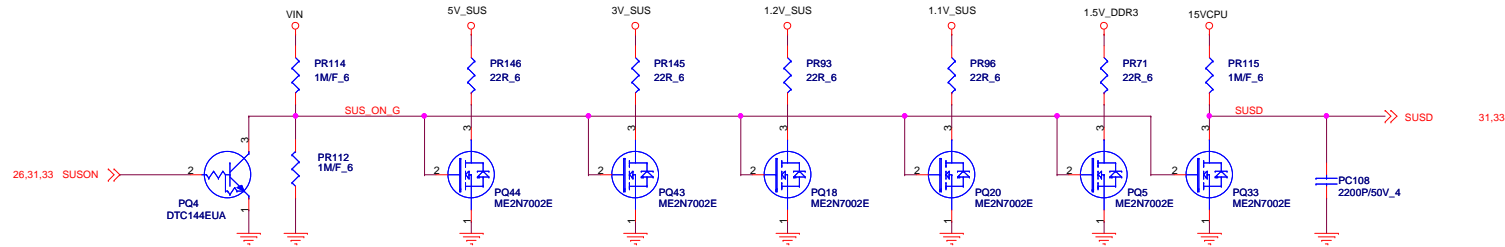
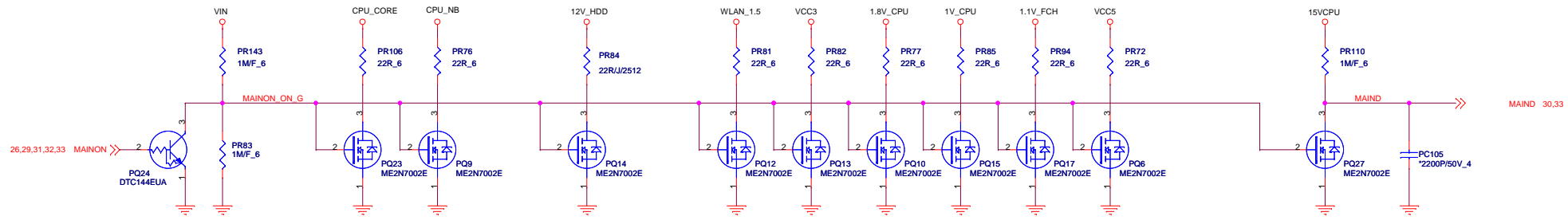


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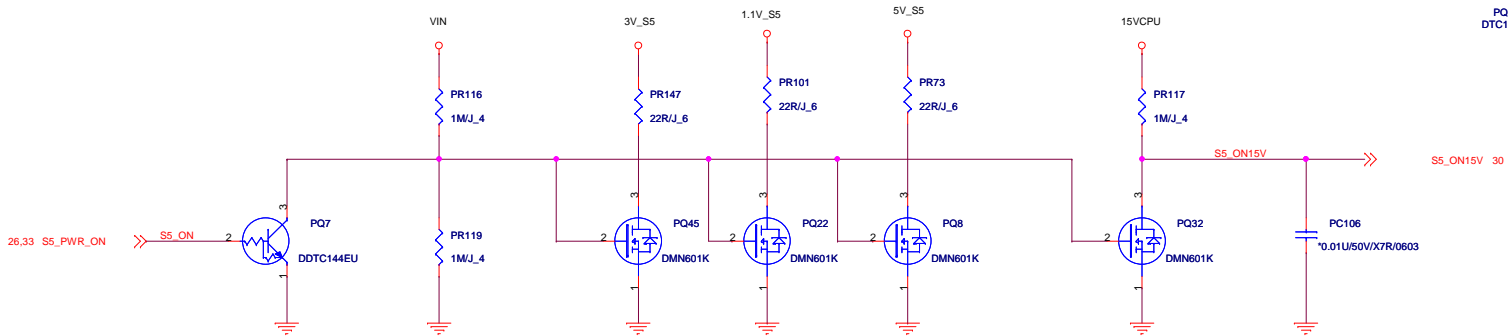


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| | | |
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VDDIO_33_S (3V_S5) power-rail ramp-down time must be more than 300 μ s



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| | | | | | | | | | |
|------------|--|---|--|--------------------------|--|----------|--|----|--|
| 5 | | 4 | | 3 | | 2 | | 1 | |
| DATE | | NZ3B Schematic file | | NZ3B Board file | | Revision | | 36 | |
| 2010/07/2 | | NZ3B-0702.dsn | | danz3bmb6a0-a-sandra.brd | | A | | | |
| 2010/07/23 | | NZ3B_0723.dsn | | danz3bmb6b0-b-sammy.brd | | B | | | |
| DATE | | Schematic Change Description | | | | | | | |
| 2010/07/20 | | Connect ADOGND and digital_ground by AR1, AR21, AR17,AR25, AR22 and AR19 on page 21. | | | | | | | |
| | | Remove R238 , add u28 at lan on page 22. | | | | | | | |
| | | Swap USBP+11 and USBP-11, swap USBP+13 and USBP-13 on page 25 | | | | | | | |
| | | Remove PR175 on page 29 | | | | | | | |
| | | the PU6 and PU10 power source change from 3.3V_SUS to 1.5V_DDR3 on page 33 | | | | | | | |
| | | the PQ19 gate source change from mainon to mainD on page 33 | | | | | | | |
| | | Modify net name from 15VPCU to 15VCPU on page 35 | | | | | | | |
| 2010/07/30 | | Change Con2 from 40 pin to 30 pin and CN9 change type from right angle to vertical on page 20 | | | | | | | |
| | | Change CN27 and CN28 from right angle type to vertical type on page 21 | | | | | | | |
| | | Change CN14 from 4 pin to 2 pin on page 24 | | | | | | | |
| | | Change CN2 from right angle type to vertical type on page 25 | | | | | | | |
| 2010/08/10 | | Add R403 for EDID GPIO on page 12 | | | | | | | |
| | | Correct ROM recovery connect net on page 13 | | | | | | | |
| | | Add panel discharge circuit for panel power sequence on page 20 | | | | | | | |
| | | Change EDID power to 3V_P and 5V_SUS on page 20 | | | | | | | |
| | | Change Card reader connect(CN13) for ESD issue on page 23 | | | | | | | |
| | | Add U30,U31,U32 for ESD issue on page 25 | | | | | | | |
| | | Add COM port(CN50) and change power_led1/2 net on page 26 | | | | | | | |
| | | Add R87 for VADJ reserve on page 26 | | | | | | | |
| | | Delete AUX pair coupling cap on page 28 | | | | | | | |
| | | Change U24 to ANX3110 on page 28. | | | | | | | |
| | | Modify CPU core relate circuit by Power demand on page 34 | | | | | | | |
| | | Add C540,C542.C534 ~ C540 on page 18 and 24 . | | | | | | | |
| 2010/10/6 | | Delete Thermal chip for CPU on page 10 | | | | | | | |
| | | Connect SIC/SID between CPU and EC on page 10&26 | | | | | | | |
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| | |
|------------|--|
| 2010/10/6 | Add R214 to pull high the SPI_CS#_R on page 13 |
| | Change RLT8105E to RTL8111E, use to co-layout function (Add L14)on page 22 |
| | Delete R251 and add R230 for Lan power delay on page 22 |
| | Add Q23 for WL_EN function on page 24 |
| | Add R193 for LVDS 8B on page28 |
| | Add PQ55 and PQ56 for WL_EN function on page 31 |
| | Change PR36 from 3.4K to 4.02K for 1V_CPU to 1.05V on page 32 |
| | Change PR37 from 10.2K to 10K for 1.5V_DDR on page 31 |
| 2010/11/3 | Change DP_VARY_BL connect on page 10 & 28 |
| | Delete U18,U19 on page 10 |
| | Change U6 AND gate input for DDR_SYS_SHDN# on page 14 |
| | Add C278,C279,C280,C282 for USB port on page 25 |
| | Add C543,C544 for web cam lag issue on page 25 |
| | Change VADJ connect on page 20 |
| | Delete U3 on page 26 |
| | Change CN8 VCC3 net on page 24 |
| | Change PQ11 control signal to MAINON on page 31 |
| 2010/11/15 | Add C541,C542 and change value to 1000pF for EMI on page 24 |
| | Add C534 to C540 and change value to 1000pF for EMI on page 18 |
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